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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/609,106	06/27/2003	Randy D. Redd	137798	9238

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EXAMINER	
SMOOT, STEPHEN W	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 11/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/609,106	REDD ET AL.	
	Examiner	Art Unit	
	Stephen W. Smoot	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 June 2003 and 27 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) *1-9* is/are withdrawn from consideration.

5)☒ Claim(s) *23-27* is/are allowed.

6)☒ Claim(s) *10,12,14 and 20-22* is/are rejected.

7)☒ Claim(s) *11,13 and 15-19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6-27-03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office action is in response to application papers filed on 27 June 2003 and to applicant's election filed on 27 August 2004.

Election/Restrictions

1. Applicant's election with traverse of Group II, claims 10-27, in the reply filed on 27 August 2004 is acknowledged. The traversal is on the grounds that the two inventions are related (i.e. they are not "independent" inventions and, accordingly, are not in compliance with 35 USC 121). This is not found persuasive because the statute uses the language "independent and distinct" and there is no indication of intent by Congress to change the substantive law on the subject of restriction with regard to dependent inventions that are patentably distinct, which had long been an established practice by the Office prior to the enactment of 35 USC 121 in 1952 (see MPEP section 802.01). Further, in the restriction requirement it was shown that the two inventions were distinct and the applicant made no adequate effort to argue that they are not.

The requirement is still deemed proper and is therefore made FINAL.

2. Claims 1-9 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected invention, there being no allowable generic or linking claim.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Method of Manufacturing a Semiconductor Component that Includes Self-Aligning a Gate Electrode to a Field Plate.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 10, 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Kerber (US 5,925,919).

Referring to Figs. 1-4 and column 3, lines 4-47, Kerber discloses a process for producing a CMOS semiconductor structure that includes the following features:

- A semiconductor substrate (1) is provided;
- A gate oxide layer (2) is formed over the substrate (1);
- A polysilicon layer (3) is formed over the gate oxide layer (2);
- A nitride layer (4) and a field oxide layer (5) are sequentially formed over the polysilicon layer (3);
- An opening (6) is etched through the field oxide layer (5), the nitride layer (4), and the polysilicon layer (3) as shown in Fig. 1;
- Field plates (12, 13) are then formed over the gate oxide layer (2) by laterally isotropically etching the exposed polysilicon layer (3) as shown in Fig. 2;
- A nitride dielectric layer (7) is conformally deposited over the opening and covers the exposed portions of the field plates (12, 13) as shown in Fig. 3;
- The nitride dielectric layer (7) is isotropically etched so that the field plates (12, 13) remain laterally covered with a dielectric (14) (i.e. spacers) as shown in Fig. 4;
- The exposed gate oxide (2) is removed and replaced with another gate oxide layer (8) as shown in Fig. 4; and
- A polysilicon gate electrode (9) is deposited between the field plates (12, 13) as shown in Fig. 4.

These are all of the limitations set forth in claims 10, 14 of the applicant's invention.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kerber (US 5,925,919) as applied to claim 10 above, and further in view of Calafut et al. (US 5,767,550) and Wolf and Tauber.

As shown above, Kerber anticipates claim 10 of the applicant's invention. However, Kerber lacks the further limitations to claim 10 set forth in claim 12, which are the formation of a semiconductor layer above the semiconductor substrate and then the formation of the first dielectric layer above the semiconductor layer. Calafut et al. teach the growth of an N- epitaxial layer (1002) on an N+ substrate (1001) followed by the formation of a gate oxide layer (1003) (see Fig.10 and column 7, lines 39-47).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Kerber and Calafut et al. in order to form an epitaxial layer, as taught by Calafut et al., between the substrate and gate oxide of Kerber. Wolf and Tauber recognize that fabricating MOS devices using

epitaxial layers has numerous advantages including accurate control of doping concentrations (see page 124).

8. Claims 20, 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kerber (US 5,925,919) as applied to claim 10 above, and further in view of Green et al. (US 2004/0021182 A1).

As shown above, Kerber anticipates claim 10 of the applicant's invention. However, Kerber lacks the further limitations to claim 10 set forth in claims 20, 22, which are a separation between gate electrode and field plate that is between 20 and 400 nanometers (claim 20) and a field plate that comprises titanium tungsten nitride (claim 22). Green et al. teach that a transistor operating at room temperature has a constant breakdown voltage for a gate to field plate spacing of up to about 0.4 microns (i.e. 400 nm) (see Fig. 7 and paragraph [0026]). Green et al. further teach that titanium tungsten nitride can be used as a field plate material (see paragarph [0005]).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Kerber and Green et al. in order to keep the separation between the gate electrode and the field plate of Kerber below 400 nm, as taught by Green et al., because Green et al. recognize that transistors will have a constant room temperature breakdown voltage for this amount of separation (see paragraph [0026]). Further, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Kerber and Green et al. in order to substitute titanium tungsten nitride, as taught by

Green et al., for the polysilicon field plate of Kerber, because Green et al. recognize that titanium tungsten nitride is a known field plate material that is used in self-aligned processes (see paragraph [0005]).

9. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kerber (US 5,925,919) as applied to claim 10 above.

As shown above, Kerber anticipates claim 10 of the applicant's invention and also discloses laterally isotropically etching the exposed polysilicon layer (3) as a step in forming the field plates (12, 13). However, Kerber lacks the further limitation to claim 10 set forth in claim 21, which is to shorten the length of the field plate to between 300 and 2000 nanometers.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to optimize the field plate of Kerber by shortening its length to be between 300 and 2000 nanometers through routine experimentation unless the applicant can show that their claimed range achieves unexpected results (see *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990).

Allowable Subject Matter

10. Claims 11, 13, 15-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form to include all of the limitations of the base claim and any intervening claims.

11. Claims 23-27 are allowed.

12. The following is a statement of reasons for the indication of allowable subject matter:

- Claim 11 would be allowable because the prior art of record does not teach or suggest, in combination with the other claim limitations, a method of manufacturing a semiconductor component that includes the step of self-aligning a gate electrode to a field plate, wherein the gate electrode is formed between two ohmic contact regions after the step of forming the ohmic contact regions;
- Claim 13 would be allowable because the prior art of record does not teach or suggest, in combination with the other claim limitations, a method of manufacturing a semiconductor component that includes the step of self-aligning a gate electrode to a field plate, further combined with the step of forming a gate recess in a semiconductor layer that is formed above a semiconductor substrate;
- Claims 15-16, 19 would be allowable because the prior art of record does not teach or suggest, in combination with the other claim limitations, a method of manufacturing a semiconductor component that includes the step of self-aligning a gate electrode to a field plate, further combined with the step of forming a second dielectric that includes an aluminum nitride layer;
- Claims 17-18 would be allowable because the prior art of record does not teach or suggest, in combination with the other claim limitations, a method of

manufacturing a semiconductor component that includes the step of self-aligning a gate electrode to a field plate, further combined with the step of forming a T-gate electrode that has a titanium tungsten nitride layer; and

- Claims 23-27 are allowed because the prior art of record does not teach or suggest, in combination with the other claim limitations, a method of manufacturing a semiconductor component that includes the steps of forming a field plate that comprises titanium tungsten nitride above a first dielectric layer, forming a second dielectric layer above the field plate and also above two ohmic contact regions, forming a hole in the second dielectric and also between the two ohmic contact regions, wherein a portion of the field plate is removed, and forming a T-gate electrode in and over the hole, wherein a spacer isolates the field plate from the T-gate.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Gill, Young, Wu, Hebert et al., and Baek teach methods of forming semiconductor structures that utilize field plates.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen W. Smoot whose telephone number is 571-272-1698. The examiner can normally be reached on M-F (8:00 am to 4:30 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sws

Stephen W. Smoot
Patent Examiner
Art Unit 2813